CLAIMS

1. – 15. (Canceled).

16. (Previously Presented) A method of conserving power in a computer processor, comprising:

reading a software-accessible control register;

determining an idle status of a subunit of the computer processor based on the control register;

providing a clock signal to the subunit based on the determined idle status; and

providing a power voltage to the subunit based on the determined idle status and a power management signal.

17. (Previously Presented) The method as recited in Claim 16, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

18. (Previously Presented) The method as recited in Claim 17, wherein determining the idle status comprises reading the at least one bit associated with the at least one subunit of the computer processor.

19. (Previously Presented) The method as recited in Claim 16, further comprising setting one or more of a plurality of bits in the control register based on an idle status of a subunit of the computer processor.

20. (Previously Presented) The method as recited in Claim 16, wherein the computer processor comprises data flow circuitry comprising a plurality of data flow sections, at least one data flow section configured as a subunit of the computer processor.

21. (Previously Presented) The method as recited in Claim 16, wherein the computer processor comprises upper and lower bit data register circuitry portions, at least the upper bit data register circuitry portion configured as a subunit of the computer processor.

22. (Previously Presented) The method as recited in Claim 16, wherein:

the computer processor comprises partitioned dataflow registers comprising a lower portion register consistent in size with the lowest instruction width software to be used in the computer processor; and

the control register comprises an architected control register bit indicating the width of the greatest instruction width presently being used by the computer processor.

23. (Previously Presented) The method as recited in Claim 16, wherein the computer processor comprises partitioned arithmetic logic units (ALUs), comprising an upper ALU and a lower ALU, at least the upper ALU configured as a subunit of the computer processor.

24. (Previously Presented) The method as recited in Claim 16, wherein the computer processor comprises a floating point logic unit (FPU), the FPU configured as a subunit of the computer processor.

25 – 36. (Cancelled)